

and V_T . The threshold voltage V_T of a MOS transistor is varied by varying the substrate voltage V_{BB} thereof. For example, as seen from FIG. 78B, in the case of NMOS, if V_{BB} is increased in its negative direction, the threshold voltage V_T is enhanced whereas if V_{BB} is decreased in the same direction, V_T is lowered. In order to operate a sense amplifier at a low voltage (1.0 V or so) and also at a high speed, the threshold voltage may be lowered. To this end, in accordance with this embodiment, as seen from FIG. 78A, the threshold voltage of a MOS transistor in diode-connection is monitored through its constant current driving, the monitored threshold voltage is compared with the reference voltage V_R by the comparator circuit COMP, and an output voltage from the V_{BB} generating circuit is controlled by the output from the comparator circuit so that the threshold voltage of the monitoring MOS transistor equals the reference voltage V_R . Thus, even if the threshold voltage of the MOS transistor is located at a point b higher than a point a indicative of an optimum value due to fabrication variation, by lowering V_{BB} to $VB1$, the threshold voltage can be shifted so as to be equal to V_R . Further, if the threshold voltage is located at a lower point (point c), by enhancing V_{BB} to $VB2$, the threshold voltage can be also shifted to a point e so as to be equal to V_R . Therefore, in accordance with this embodiment, a sense amplifier stabilized against fabrication variation can be provided. Further, by setting V_R at (a point f) lower than (the standard point a) during the operation time and setting it at (a higher point g) during the stand-by time, the high speed operation during the operation time and the reduced power consumption can be simultaneously realized. Moreover, with the well provided with the same circuit, during the operation time, V_R is set negative for NMOS and positive for PMOS in order to place their threshold voltage in a depletion type whereas during the stand-by time, it is set positive for NMOS and negative for PMOS to place their threshold voltage in an enhancement type which is normal. Thus, the high speed operation and low voltage amplitude can be further advanced. In the case where the substrate voltage is required to be varied at a high speed because the operation cycle is short, the triple well structure may be used to separate the substrate part corresponding to the sense amplifier section whereby reduced power consumption can be realized also for the V_{BB} generating circuit.

FIG. 78C shows a concrete structure of FIG. 78A. In FIG. 78C, QB1 and QB2 are MOS transistors for monitoring; QB3 to QB8 constitute a comparator; OSC is an oscillating circuit for the V_{BB} generating circuit; and INV1, INV2, C2, C3 and QB9 to QB12 constitute the V_{BB} generating circuit. It should be noted that two stages of monitoring MOS transistors are connected for the purpose of an optimum bias for the comparator circuit. Correspondingly, V_R is required to be twice as large as an objective threshold voltage. Incidentally, the number of the stages of the monitoring transistors is not limited but may be any number which permits an input voltage for the comparator circuit to be optimized. Further, the rectifying circuit (C2, C3 and QB9 to QB12) in the V_{BB} generating circuit is adapted to generate a double voltage in order to extend the control range of the threshold voltage, but this may be changed in accordance with the rate of change for the operation voltage of the sense amplifier or the substrate voltage. In this way, in accordance with this embodiment, the threshold voltage in the sense amplifier can be stabilized regardless of fabrication variation and also can be varied in the operation time and stand-by time so that DRAM with the characteristics of a high speed and reduced power consumption can be provided.

Accordingly, in accordance with this embodiment, a memory circuit which can operate at a comparatively low power supply voltage without injuring the speed performance can be realized. The idea in this embodiment can also be applied to the circuit components other than the sense amplifiers whereby an LSI memory with the performances of a high operation speed and reduced power consumption can be provided. Further, without being limited to the memory LSI, the other LSI such as a logic LSI which can operate at a comparatively low power supply voltage can also be provided. Incidentally, the gist of the present invention is that means of detecting the operation threshold voltage of the elements is provided and the threshold voltage is controlled by an output from the means so that it is an optimum value for circuit operation and so the circuit arrangement should not be limited to the arrangement mentioned above.

The present invention has been explained in relation to DRAM, but may be applied to an LSI in any form including a random access memory (RAM) (dynamic or static), a read only memory (ROM), a logic LSI such as a microcomputer, etc. Further, the elements or devices to be used may be bipolar transistors, MOS transistors, the combination thereof, or transistors made of the material e.g. GaAs other than Si.

Accordingly, in accordance with the present invention, a memory circuit which can operate at a comparatively low power supply voltage without injuring the speed performance can be realized. This memory circuit can be used as a memory for battery back-up or battery operation. The idea in this embodiment can also be applied to the circuit components other than the sense amplifiers whereby an LSI memory with the performances of a high operation speed and reduced power consumption can be provided. Further, without being limited to the memory LSI, the other LSI such as a logic LSI which can operate at a comparatively low power supply voltage can also be provided.

Further, in accordance with the present invention, one chip ULSI which can operate in accordance with a wide range of power supply voltage can be realized. Also, the ULSI with reduced power consumption can be accomplished. One chip ULSI which can correspond to a number of input/output levels can also be realized.

It is further understood by those skilled in the art that the foregoing description is preferred embodiments of the disclosed devices and that various changes and modifications may be made in the invention without departing from the spirit and scope thereof.

We claim:

1. A semiconductor device comprising:

a plurality of data line pairs, a plurality of word lines intersecting said plurality of data line pairs, memory cells located at the intersecting points, sense amplifiers each for amplifying a difference voltage of a data line pair of said plurality of data line pairs to a first voltage in a term of an amplifying operation, and a common driving line pair for driving said sense amplifiers;

wherein the voltage amplitude between said common driving line pair is made larger than the maximum value of said first voltage between the data line pair in a part of the term of the amplifying operation.

2. A semiconductor device according to claim 1:

wherein the common driving line pair is one of a plurality of common driving line pairs and, wherein the voltage of one of said common driving line pairs is boosted by boosting capacitors.

3. A semiconductor device according to claim 1 further comprising:

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first, second and third power supply lines, and three switches connecting said first, second and third power supply lines with said common driving line pair respectively;

wherein the voltage between said first and second power supply lines is larger than the voltage between said second and third power supply lines which is substantially equal to the maximum value of said first voltage between the data line pair.

4. A semiconductor device according to claim 3, wherein one of the voltages of the power supply lines is generated on the chip.

5. A semiconductor device comprising:

a plurality of data lines, a plurality of word lines intersecting the plurality of data lines, memory cells located at the intersecting points, sense amplifiers each for amplifying a memory cell signal read out on each of the data lines, common driving lines for driving said sense amplifiers, and an internal voltage generator to generate a first internal voltage;

wherein said first internal voltage is substantially an intermediate value between a first external voltage and a second external voltage when the difference between the first and second external voltages is larger than a first reference voltage, whereas the difference between the first internal voltage and one of the external voltages is made constant when the difference between the first and the second external voltages is larger than a second reference voltage.

6. A semiconductor device comprising:

a plurality of data lines, a plurality of word lines intersecting the plurality of data lines, memory cells located at the intersecting points, sense amplifiers each for amplifying a memory cell signal read out on each of the data lines, and common driving lines for driving said sense amplifiers;

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wherein when said sense amplifiers start to operate, voltage of the data lines is varied to effectively boost an absolute value of the gate-source voltage of transistors in each of the sense amplifiers.

7. A semiconductor device according to claim 6, wherein said voltage of the data lines is boosted by capacitors.

8. A semiconductor device comprising:

a plurality of data lines, a plurality of word lines intersecting the plurality of data lines, memory cells located at the intersecting points, sense amplifiers each for amplifying a memory cell signal read out on each of the data lines, and common driving lines for driving said sense amplifiers;

wherein said sense amplifiers operate with a voltage amplitude higher than that of the data lines and each of said sense amplifiers includes an inverter which operates with a voltage amplitude as that of the data lines.

9. A semiconductor device comprising:

a plurality of data lines, a plurality of word lines intersecting the plurality of data lines, memory cells located at the intersecting points, sense amplifiers each for amplifying a memory cell signal read out on each of the data lines, and common driving lines for driving said sense amplifiers;

wherein a threshold voltage of each of the transistors in each of the sense amplifiers is varied in accordance with the operating condition of the sense amplifiers.

10. A semiconductor device according to claim 9, wherein said threshold voltage is varied dynamically.

11. A semiconductor device according to claim 10, wherein said threshold voltage is varied in range including 0 V.

12. A semiconductor device according to claim 10, wherein said threshold voltage is varied by varying a substrate voltage.

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13. A semiconductor device comprising:

a first circuit block having a plurality of circuits and being operative by a first voltage which is defined by a first potential and a second potential; and

a voltage generator producing a first bias voltage which is determined with reference to the first potential and a second bias voltage which is determined with reference to the second potential,

wherein each of the plurality of circuits includes a first MISFET with a first conduction type, a second MISFET with the first conduction type, a third MISFET with a second conduction type, and a fourth MISFET with the second conduction type which are coupled in series between the first potential and the second potential, and

wherein the first bias voltage is supplied to the gate of the second MISFET and the second bias voltage is supplied to the gate of the third MISFET.

14. A semiconductor device according to claim 13,

wherein each of the plurality of circuits further includes a set of input nodes which are the gates of the first and fourth MISFETs, a first coupling node between the first MISFET and the second MISFET, a second coupling node between the third MISFET and the fourth MISFET, and a third coupling node between the second MISFET and the third MISFET,

wherein the set of input nodes are prepared to receive a set of input signals having an amplitude that is smaller than the first voltage,

wherein the first coupling node can output a first output signal having an amplitude that is smaller than the first bias voltage,

wherein the second coupling node can output a second output signal having an amplitude that is smaller than the second bias voltage, and

wherein the third coupling node can output a third output signal having an amplitude that is larger than that of the first output signal or the second output signal.

15. A semiconductor device according to claim 13,

wherein the channel conductance of the second MISFET is larger than that of the first MISFET, and

wherein the channel conductance of the third MISFET is larger than that of the fourth MISFET.

16. A semiconductor device according to claim 13,

wherein one of the plurality of circuits is an inverter circuit including the first, second, third, and fourth MISFETs,

wherein the inverter circuit further includes a set of input nodes which are the gates of the first and fourth MISFETs, a first coupling node between the first MISFET and the second MISFET, a second coupling node between the third

MISFET and the fourth MISFET, and a third coupling node between the second MISFET and the third MISFET,

wherein the set of input nodes are prepared to receive a set of input signals having an amplitude that is smaller than the first voltage,

wherein the first coupling node can output a first output signal having an amplitude that is smaller than the first bias voltage,

wherein the second coupling node can output a second output signal having an amplitude that is smaller than the second bias voltage, and

wherein the second coupling node can output a third output signal having an amplitude that is larger than that of the first output signal or the second output signal.

17. A semiconductor device according to claim 13, further comprising a second circuit block being operative by a second voltage which is smaller than the first voltage,

wherein one of the plurality of circuits is an output circuit which receives a first signal with a first amplitude outputted from the second circuit block and outputs a second signal with a second amplitude which is larger than the first amplitude,

wherein the output circuit includes a level converter circuit which receives the first signal, a first inverter circuit which receives a set of signals outputted from the

level converter circuit, and a second inverter circuit which receives a set of signals outputted from the first inverter circuit and outputs the second signal, and

wherein each of the level converter circuit, the first inverter circuit, and the second inverter circuit includes the first, second, third, and fourth MISFETs.

18. A semiconductor device according to claim 21, wherein the first amplitude is substantially the same as the second voltage and the second amplitude is substantially the same as the first voltage.

19. A semiconductor device according to claim 13, wherein one of the plurality of circuits is a NAND circuit including the first, second, third, and fourth MISFETs,

wherein the NAND circuit further includes a fifth MISFET with the first conduction type having a source-drain path that is coupled in parallel with the source-drain path of the first MISFET and a sixth MISFET with the second conduction type having a source-drain path that is coupled between one end of the source-drain path of the fourth MISFET and the second potential,

wherein the NAND circuit further includes a set of first input nodes which are the gates of the first and fourth MISFETs, a set of second input nodes which are the gates of fifth and sixth MISFETs, a first coupling node between the first MISFET and the second MISFET, a second coupling node

between third MISFET and the fourth the MISFET, and a third coupling node between the second MISFET and the third MISFET,

wherein the set of first input nodes are prepared to receive a set of first input signals having an amplitude that is smaller than the first voltage,

wherein the set of second input nodes are prepared to receive a set of second input signals having an amplitude that is smaller than the first voltage,

wherein the first coupling node can output a first output signal having an amplitude that is smaller than the first bias voltage,

wherein the second coupling node can output a second output signal having an amplitude that is smaller than the second bias voltage, and

wherein the second coupling node can output a third output signal having an amplitude that is larger than that of the first output signal or the second output signal.

20. A semiconductor device according to claim 13,

wherein one of the plurality of circuits is a tri-state output buffer circuit including a NAND circuit, a NOR circuit, and an output driver, and

wherein each of the NAND circuit, the NOR circuit, and the output driver includes the first, second, third, and fourth MISFETs.

21. A semiconductor device according to claim 20,

wherein the NAND circuit further includes a set of first input nodes which are the gates of the first and fourth MISFETs of the NAND circuit to which a set of first input signals are supplied, and a first output node from which a first output signal is outputted,

wherein the NOR circuit further includes a set of second input nodes which are the gates of the first and fourth MISFETs of the NOR circuit to which a set of second input signals are supplied, and a second output node from which a second output signal is outputted,

wherein the output driver further includes a set of third input nodes which are the gates of the first and fourth MISFETs of the output circuit, and a coupling node between the second and third MISFETs,

wherein the first output node is coupled to one of the set of third input nodes and the second output node is coupled to another one of the set of the third input nodes, and

wherein the coupling node of the output driver can output a third output signal having an amplitude that is larger than that of the first output signal or the second output signal.

22. A semiconductor device according to claim 21,

wherein the amplitude of the third output signal is substantially the same as the first voltage.

23. A semiconductor device according to claim 13,

wherein said semiconductor device is formed on a chip,
wherein one of the plurality of circuits is an input
circuit which receives an input signal from an outside of the
chip and includes the first, second, third, and fourth
MISFETs,

wherein the input circuit further includes a fifth MISFET
with the first conduction type having one end of the source-
drain path that is coupled to the gate of the first MISFET and
having a gate that is coupled to the gate of the second
MISFET, and a sixth MISFET with the second conduction type
having one end of the source-drain path that is coupled to the
gate of the fourth MISFET and having a gate that is coupled to
the gate of the third MISFET,

wherein the input circuit further includes a first
coupling node between the first MISFET and the second MISFET,
and a second coupling node between the third MISFET and the
fourth MISFET,

wherein another end of the source-drain path of the fifth
MISFET and another end of the source-drain path of the sixth
MISFET are coupled together and the input signal is supplied
thereto,

wherein the first coupling node can output a first output
signal having an amplitude that is smaller than the first bias
voltage, and

wherein the second coupling node can output a second output signal having an amplitude that is smaller than the second bias voltage.

24. A semiconductor device according to claim 23, wherein the amplitude of the input signal is substantially the same as the first voltage.

25. A semiconductor device according to claim 13, wherein the first bias voltage is defined by the first potential and a third potential and the second bias voltage is defined by the second potential and a fourth potential, and wherein the first potential is higher than the second potential, the third potential is lower than the first potential, and the fourth potential is higher than the second potential.

26. A semiconductor device according to claim 25, wherein the first potential has a first changing rate according to the variation of the first voltage and the second potential has a second changing rate according to the variation of the first voltage,

wherein when the first voltage is in a first predetermined voltage range, the third potential has a third changing rate according to the variation of the first voltage and the fourth potential has a fourth changing rate according to the variation of the first voltage, and

wherein the third changing rate is larger than the fourth changing rate.

27. A semiconductor device according to claim 26,
wherein the first changing rate is larger than the second changing rate, and

wherein the third changing rate is proportional to the first changing rate, and the fourth changing rate is proportional to the second changing rate.

28. A semiconductor device according to claim 27,
wherein the third changing rate is substantially equal to the first changing rate, and the fourth changing rate is substantially equal to the second changing rate.

29. A semiconductor device according to claim 28,
further comprising a second circuit block being operative by a second voltage which is smaller than the first voltage,

wherein a thickness of a gate insulator layer of said MISFETs in said first circuit block is substantially the same as that of MISFETs included in said second circuit block.

30. A semiconductor device according to claim 29,
wherein the first conduction type is a P-channel and the second conduction type is an N-channel, and

wherein said semiconductor device is a microprocessor LSI in a chip.

31. A semiconductor device according to claim 26,

wherein when the first voltage is in a second predetermined voltage range which is larger than the first predetermined voltage range, the third potential has a fifth changing rate according to the variation of the first voltage and the fourth potential has a sixth changing rate according to the variation of the first voltage, and

wherein the fifth changing rate is smaller than the third changing rate and sixth changing rate is larger than the fourth changing rate.

32. A semiconductor device according to claim 31, wherein both the fifth and sixth changing rates are half of the first changing rate.

33. A semiconductor device according to claim 31, wherein the second predetermined voltage range is an aging operation voltage range for said semiconductor device.

34. A semiconductor device according to claim 33, wherein the first conduction type is a P-channel and the second conduction type is an N-channel.

35. A semiconductor device according to claim 34, further comprising a second circuit block being operative by a second voltage which is smaller than the first voltage,

wherein a thickness of a gate insulator layer of said MISFETs in said first circuit block is substantially the same as that of MISFETs included in said second circuit block.

36. A semiconductor device according to claim 35,

wherein said semiconductor device is a microprocessor LSI in a chip.

37. A semiconductor device according to claim 14,
wherein the first conduction type is a P-channel and the
second conduction type is an N-channel.

38. A semiconductor device according to claim 14,
further comprising a second circuit block being operative by a
second voltage which is smaller than the first voltage,

wherein a thickness of a gate insulator layer of said
MISFETs in said first circuit block is substantially the same
as that of MISFETs included in said second circuit block.

39. A semiconductor device according to claim 14,
further comprising a second circuit block being operative by a
second voltage which is smaller than the first voltage,

wherein said semiconductor device is a microprocessor LSI
chip, and

wherein the second circuit block is an internal circuit
block and the first circuit block is an interface circuit
block between the internal circuit and an outside of the
microprocessor LSI chip.

40. A semiconductor device according to claim 14,
wherein said semiconductor device is a dynamic random access
memory chip.

41. A semiconductor device according to claim 14,
further comprising a second circuit block being operative by a
second voltage which is smaller than the first voltage,
wherein said semiconductor device is a microprocessor LSI
chip,

wherein a thickness of a gate insulator layer of said
MISFETs in said first circuit block is substantially the same
as that of MISFETs included in said second circuit block, and
wherein the first voltage is an external voltage supplied
from an outside of the microprocessor LSI chip.

42. A semiconductor device comprising:
a first circuit block being operative by a first voltage;
and

a second circuit block being operative by a second
voltage which is larger than the first voltage and is defined
by a first potential and a second potential,

wherein said second circuit block includes an output
circuit which receives a first signal outputted from the first
circuit block and outputs a second signal having an amplitude
that is larger than that of the first signal,

wherein the output circuit further includes a level
converter circuit which receives the first signal, a first
inverter circuit, and a second inverter circuit,

wherein the level converter circuit includes a 1st
MISFET, a 2nd MISFET, a 3rd MISFET, and a 4th MISFET which are

coupled in series between the first potential and the second potential,

wherein the level converter circuit includes a 5th MISFET, a 6th MISFET, a 7th MISFET, and an 8th MISFET which are coupled in series between the first potential and the second potential,

wherein the level converter circuit includes a first coupling node between the 5th MISFET and the 6th MISFET and a second coupling node between the 7th MISFET and the 8th MISFET,

wherein the gates and drains of the 1st and the 5th MISFETs are cross-coupled together,

wherein the first signal is supplied to the gate of the 4th MISFET and inverted the first signal is supplied to the gate of the 8th MISFET,

wherein the first inverter circuit includes a 9th MISFET, a 10th MISFET, an 11th MISFET, and a 12th MISFET which are coupled in series between the first potential and the second potential,

wherein the first inverter circuit further includes a third coupling node between the 9th MISFET and the 10th MISFET and a fourth coupling node between the 11th MISFET and the 12th MISFET,

wherein the gate of the 9th MISFET is coupled to the first coupling node and the gate of the 12th MISFET is coupled to the second coupling node,

wherein the second inverter circuit includes a 13th MISFET, a 14th MISFET, a 15th MISFET, and a 16th MISFET which are coupled in series between the first potential and the second potential,

wherein the second inverter circuit further includes a fifth coupling node between the 14th MISFET and the 15th MISFET,

wherein the gate of the 13th MISFET is coupled to a third coupling node and the gate of the 16th MISFET is coupled to the fourth coupling node, and

wherein the fifth coupling node can output the second signal.

43. A semiconductor device according to claim 42, further comprising a voltage generator producing a first bias voltage which is determined with reference to the first potential and a second bias voltage which is determined with reference to the second potential,

wherein the first bias voltage is supplied to the gates of the 2nd, 6th, 10th, and 14th MISFETs and the second bias voltage is supplied to the gates of the 3rd, 7th, 11th, and 15th MISFETs.

44. A semiconductor device according to claim 43,

wherein the channel conductance of the 2nd, 6th, 10th, and 14th MISFETs is larger than that of the 1st, 5th, 9th, and 13th MISFETs, and

wherein the channel conductance of the 3rd, 7th, 11th, and 15th MISFETs is larger than that of the 4th, 8th, 12th and 16th MISFETs.

45. A semiconductor device according to claim 43,

wherein the amplitude of the first signal is substantially equal to the first voltage and an amplitude of the second signal is substantially equal to the second voltage.

46. A semiconductor device according to claim 43,

wherein the first bias voltage is defined by the first potential and a third potential and the second bias voltage is defined by the second potential and a fourth potential,

wherein the first potential is higher than the second potential, the third potential is lower than the first potential, and the fourth potential is higher than the second potential, and

wherein the first potential has a first changing rate according to the variation of the second voltage and the second potential has a second changing rate according to the variation of the second voltage,

wherein when the second voltage is in a first predetermined voltage range, the third potential has a third

changing rate according to the variation of the second voltage and the fourth potential has a fourth changing rate according to the variation of the second voltage, and

wherein the third changing rate is larger than the fourth changing rate.

47. A semiconductor device according to claim 46, wherein when the second voltage is in a second predetermined voltage range which is larger than the first predetermined voltage range, the third potential has a fifth changing rate according to the variation of the second voltage and the fourth potential has a sixth changing rate according to the variation of the second voltage, and

wherein the fifth changing rate is smaller than the third changing rate and sixth changing rate is larger than the fourth changing rate.

48. A semiconductor device according to claim 47, wherein both the fifth and sixth changing rates are half of the first changing rate.

49. A semiconductor device according to claim 47, wherein the second operating voltage range is an aging operation voltage range for said semiconductor device.

50. A semiconductor device according to claim 43, wherein the 1st, 2nd, 5th, 6th, 9th, 10th, 13th, and 14th MISFETs are P-channel MISFETs and the 3rd, 4th, 7th, 8th, 11th, 12th, 15th, and 16th MISFETs are N-channel MISFETs.

51. A semiconductor device according to claim 50,
wherein a thickness of a gate insulator layer of MISFETs
in said first circuit block is substantially the same as those
of said MISFETs included in said second circuit block.

52. A semiconductor device according to claim 51,
wherein said semiconductor device is a microprocessor LSI
chip, and

wherein the first circuit block is an internal circuit
block and the second circuit block is an interface circuit
block between the internal circuit and an outside of the
microprocessor LSI chip.